Design Of Neural Network Circuit Inside High Speed Camera Using Analog CMOS 0.35 µm Technology

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Abstract

Analog VLSI on-chip learning Neural Networks represent a mature technology for a large number of applications involving industrial as well as consumer appliances. This is particularly the case when low power consumption, small size and/or very high speed are required. This approach exploits the computational features of Neural Networks, the implementation efficiency of analog VLSI circuits and the adaptation capabilities of the on-chip learning feedback schema. High-speed video cameras are powerful tools for investigating for instance the biomechanics analysis or the movements of mechanical parts in manufacturing processes. In the past years, the use of CMOS sensors instead of CCDs has enabled the development of high-speed video cameras offering digital outputs , readout flexibility, and lower manufacturing costs. In this paper, we propose a high-speed smart camera based on a CMOS sensor with embedded Analog Neural Network.

1. Introduction

The human vision presents high capacities in terms of information acquisition (high image resolution) and information processing (high performance processing). Nevertheless, the human vision is limited because human's reactions to a stimulus are not necessarily instantaneous. The human vision presents spatial and temporal resolution limitations. More precisely, the human vision temporal resolution is close to 100 milliseconds [1]. Moreover, the fast information storage capacity of the human system is difficult to evaluate. On the other hand, the human vision system is very performant in terms of image analysis which extracts relevant information. In the last few years, technical progresses in signal acquisition [2, 3] and processing have allowed the development of new artificial vision system which equals or overpasses human capacities.

Therefore, the goal of our research is to implement embedded analog CMOS Neural Network for high speed smart camera. High speed smart camera needs : : a fast image acquisition, images with high resolution, and real-time image analysis which only keeps necessary information. Because of this, neural networks operating in a few milliseconds are required.

2. High Speed Camera Description

In order to design our high-speed smart camera, some constraints had to be respected. The first one was of course high frequency acquisition as well as embedded image processing.

Nowadays, in the context of fast imaging, CMOS image sensors present more and more advantages in comparison with CCD image sensors that we will summarize hereafter .

(i) *Random access to pixel regions:* in CMOS image sensors, both the detector and the readout amplifier are part of each pixel. This allows the integrated charge to be converted into a voltage inside the pixel, which can then be read out over X-Y wires (instead of using a charge shift register like in CCDs). This column and row addressability is similar to common RAM and allows region-of-interest (ROI) readout.

(ii) *Intrapixel amplification and on-chip ADC (analog to digital converter) produce faster frame rates*.

(iii) *No smear and blooming effects:* CCDs are limited by the blooming effect because charge shift registers can leak charge to adjacent pixels when the CCD register overflows, causing bright lights. In CMOS image sensors, the signal charge is converted to a voltage inside the pixel and read out over the column bus, as in a DRAM (dynamic random access memory).With this architecture, it is possible to add an antiblooming protection in each pixel. Smear, caused by charge transfer in a CCD under illumination, is also avoided.

(iv) *Low power:* CMOS pixel sensor architectures consume much less power—up to 100 x less power—than CCDs. This is a great advantage for portable high speed cameras.

2.1. High Speed Camera Systems

As in a traditional image sensor, the core of the chip presented ini this paper constructed of a two-dimensional (2-D) pixel array, here of 64 columns and 64 rows with random pixel ability, and some peripheral circuits. It contains about 160 000 transistors on a 3.675 mm x 3.775 mm die. The main chip characteristics are listed in Table 1.

Table 1 : Chip Characteristics

Technology	0.35 µm 2-poly 4-metal CMOS
Array size	64 x 64
Chip size	11 mm^2
Number of transistors	160 000
Number of transistors / pixel	38
Pixel size	35 µm x 35µm
Sensor Fill Factor	25 %
Dynamic power consumption	110 mW
Supply voltage	3.3 V
Frame rate	10 000 fps

Each individual pixel contains a photodiode for the light to-voltage transduction and 38 transistors integrating all the analog circuitry dedicated to the image processing algorithms. This amount of electronics includes a preloading circuit, two *Analog Memory, Amplifier and Multiplexer* structures ($[AM]^2$) and an *Analog Arithmetic Unit* (A^2U) based on a four-quadrant multiplier architecture. The full pixel size is 35 µm x 35µm with a 25 % fill factor. Fig. 1 shows a block diagram of the proposed chip. The architecture of the chip is divided into three main blocks as in many circuits widely described in the literature. First, the array of pixels (including photodiodes with their associated circuitry for performing the analog computation) is placed at the center. Second, placed below the chip core are the readout circuits with the three asynchronous output buses: the first one is dedicated to the image processing results whereas the other two provide parallel outputs for full high rate acquisition of raw images. Finally, the left part of the sensor is dedicated to a row decoder for addressing the successive rows of pixels. The pixel values are selected one row at a time and read out to vertical column buses connected to an output multiplexer. The chip also contains test structures used for detailed characterization of the photodiodes and processing units. These test structures can be seen on the bottom left of the chip.

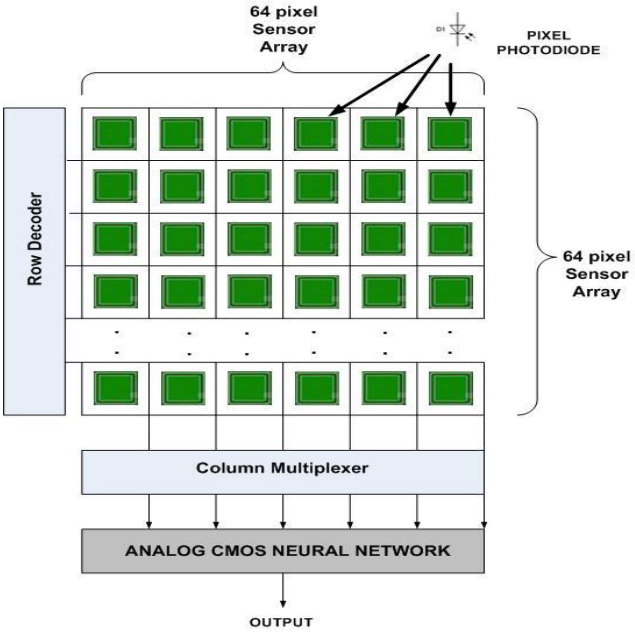

Figure 1. Block Diagram of the Chip

In Figure 1 shows of block diagram that have a speed camera taking a picture of 10,000 frames / second. Block the camera has been designed by Jerome Dubois is the matrix of 64x64 pixels or 4096 pixels. The process of catching an object pixel by using the decoder and then strengthened by column multiplexer. In Jerome design, he create the image processing that uses low-level basic image processing such as edge detection using Sobel and Lappacian. [9]

3. Embedded Analog Cmos Neural Network

Conception of structures in CMOS technology that demand low power and low silicon area consumption have been widely investigated in the implementation of analog neural networks in VLSI integrated circuits. Feedforward MLP networks' building blocks require CMOS multipliers for implementing the synapses, operational amplifier as current voltage converter and sigmoid generator for activation function circuits. A larger scale of integration of such networks happens at the expense of simpler and, as a result, nonlinear synaptical blocks. Regarding these aspects it becomes advisable to derive suitable expressions to adjust the back-propagation algorithm and deal with these nonlinearities [5].

The synapses in a neural network can be realized by analog multipliers if the inputs and the weights can be represented by voltages. An illustrative synapse circuit which is a modified version of the well known Gilbert multiplier is shown in Figure. 1. The inputs are in the form of voltage differences and are denoted by X+*x*, X-x and Y+y and Y-y. The output of the original Gilbert multiplier is a current difference and this difference is

converted to a single ended current (*Z*) through current mirrors. This improves the linearity of the multiplier as well as providing easy interfacing to the following circuitry. Using voltage input-current output synapse for analog neural network is very suitable for VLSI implementation since the actual signals from outside are mostly in voltage form, and the summing operation on synapse output can performed by connecting the synapse output together.

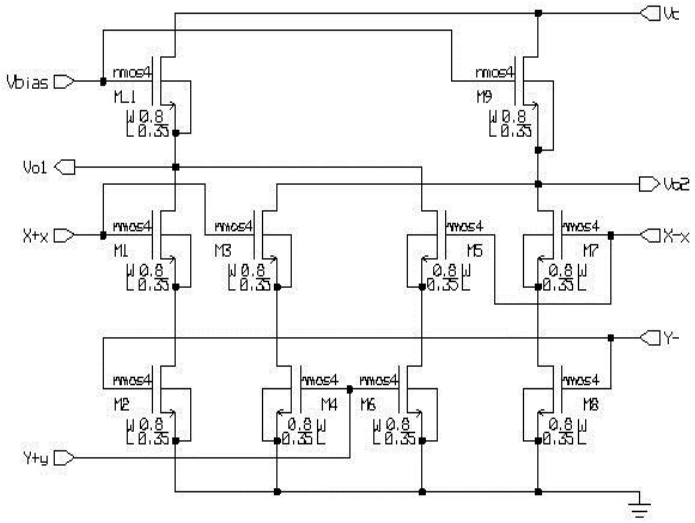

Figure 2. Analog CMOS Multiplier

The use of current-output synapses enables the summation of those currents by simply connecting them together at the input of the neuron. This current sum can be converted to voltage by using an opamp and a resistor as a current-to-voltage converter. The circuit diagram of the opamp is given in figure 5.

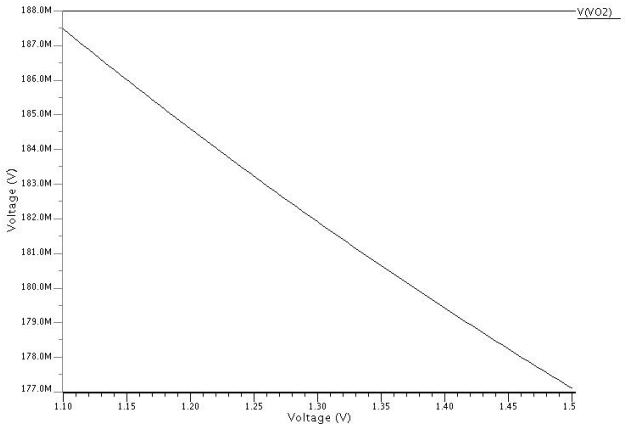

Figure 3. DC Response for signal X with values range 1.3 V- 1.5 V.

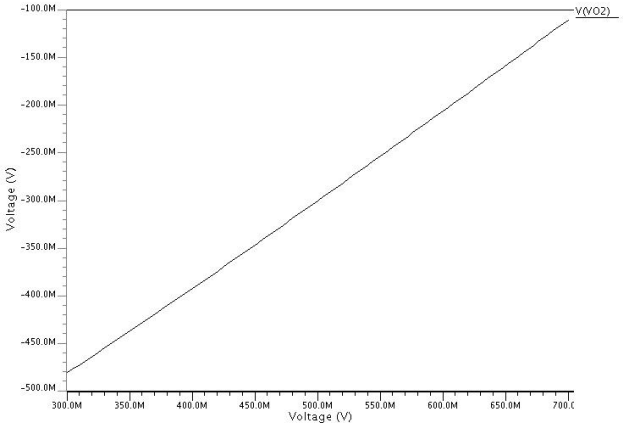

Figure 4. DC Response for signal Y with values range 0.7 V-1.3 V.

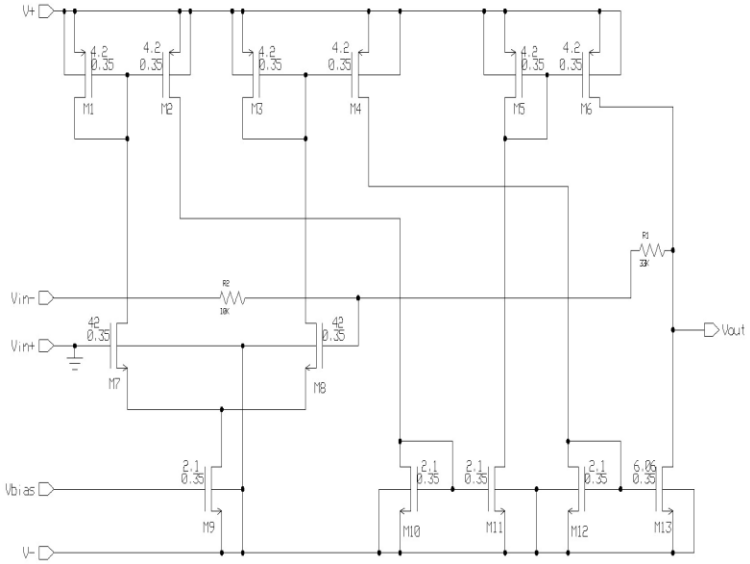

Figure 5. Operational Amplifier

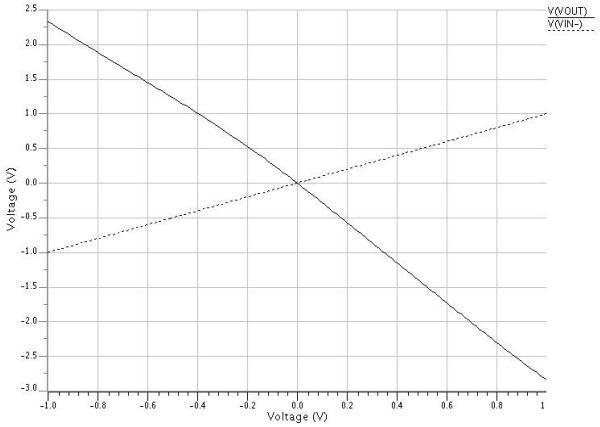

Figure 6. Opamp simulation

A sigmoid generator is used after the opamp to generate the activation for the neuron.

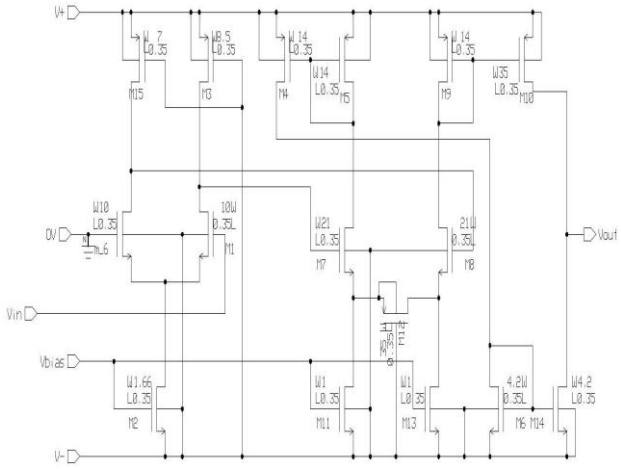

Figure 7. Sigmoid Generator

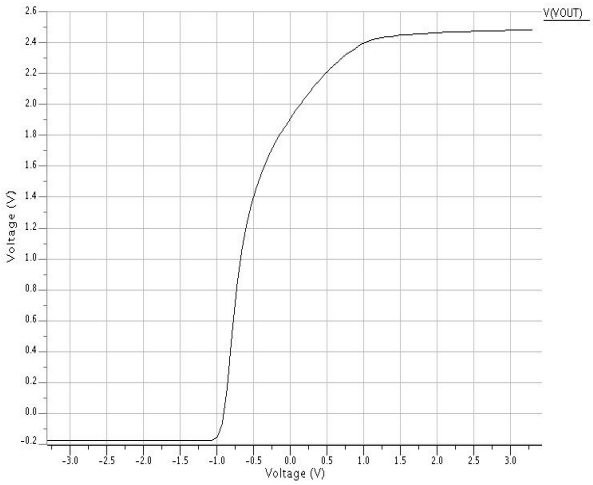

Figure 8. Sigmoid simulation

Designs and simulation of the analog neural network circuits described above are using mentor graphic with AMS technology 0.35 μm.

4. Conclusion

In this article we design analog neural network using analog CMOS 0.35 μm technolgy . All design units using Mentor Graphic. in For the future work, we wish to implement new training algorithm for high speed smart camera.

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