Design and Analysis of Three-Phase Three-Level PWM Inverter

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Abstract – Design of three-phase three level PWM inverter and analysis of the output current harmonics are presented in this paper. The three-level inverter is designed to supply three-phase load and it is controlled by FPGA under several modulation techniques (Sinusoidal PWM and Third Harmonic Injection PWM). Selection of semiconductor switches and other component of the inverter are described. Inverter output current harmonics under several modulation techniques will be analysed and compared.

Keywords : Inverter, Three-Level, Harmonics, Sinusoidal PWM, Third Harmonic Injection PWM

I. INTRODUCTION

Concept of multilevel inverter has been developed since many years for several purposes in industial applications. One popular application of multilevel inverter is for static VAR compensator in power system. Multilevel inverter is also used as motor drives, renewable energy interface, Uninterruptible Power Supply (UPS) and on Flexible AC Transmission System (FACTS) [1].

Multilevel system is popular because of its advantages, the inverter can produce medium or high AC voltage by using low switching frequency. By using low switching frequency, switching losses is decreased so that the inverter's eficiency is increased. For three-level inverter, every switch only withstand a half of total DC voltage, so *dv/dt* reduced and smaller rating of switch can be utilized [2]. Output voltage of three-level inveter are built from three state voltage combination, so the voltage wave are more like sinusiodal form than two-level inverter. Hence, the output current ripple is lower at the same switching frequency.

Recent research proved that output current ripple of three-level inverter can be minimized by injecting third harmonics to its modulation signal [3]. However, it's not have been proved by experiment but only with matemathical analysis.

In this paper, a three-level three-phase inverter is designed and recent research about minimization of output current ripple is validated. Output current ripple from several modulation technique will be analyzed and compared.

II. DESIGN OF THREE-LEVEL INVERTER

Topology of designed inverter is Neutral Point Clamped that shown at Figure 1. Specifications of designed three-phase three-level inverter are :

- O utput Voltage Rating : 220/380 Volt
- R ated Power : 5 kW
- F requency : 50 Hz
- S witching Frequency : 1000 – 10000 Hz

a. C apacitor DC Link Selection

At the DC side of inverter, capacitor is needed to filter voltage ripple from DC source. Two capacitor connected in series on neutral point where voltage fluctuation occurs. This voltage fluctuation is one factor in selecting the capacitance of capacitor. Equation (1) shows the voltage value on the DC side of inverter in linear modulation range.

$$V_{DC} = \frac{2\sqrt{2}}{\sqrt{3}\,k} V_{LL} \tag{1}$$

where V_{LL} is line-to-line voltage on the AC side inverter (380 Volt) and k is modulation index. Hence the capacitance is derived from equation below [4] :

$$Ctot = \frac{\sqrt{2}.I_R}{2\pi f_R.2E}.\frac{\overline{Vn}}{Vn} \tag{2}$$

where:

- *C tot* : Total capacitance on DC side of inverter
- *I R* : Rated Current
- *f R* : Rated Frequency
- *2 E* : Total voltage on DC side of inverter
- $\overline{Vn}$: Coefficient depend on *k*

-

n : Allowed Fluctuation voltage (3%)

from equation (1) and (2), total capacitance at the DC side of inverter is 650µF or 1300µF for each capacitor.

b.

emiconductor Switch and Clamping Diode Selection

Semiconductor switch current rating is selected from the maximum mean value of current flows at the switch. The maximum mean value of current derived with the assumption that switch is operated at square wave mode, so at a half period of positive voltage the current flow through the switch. Hence, the maximum mean value of current is :

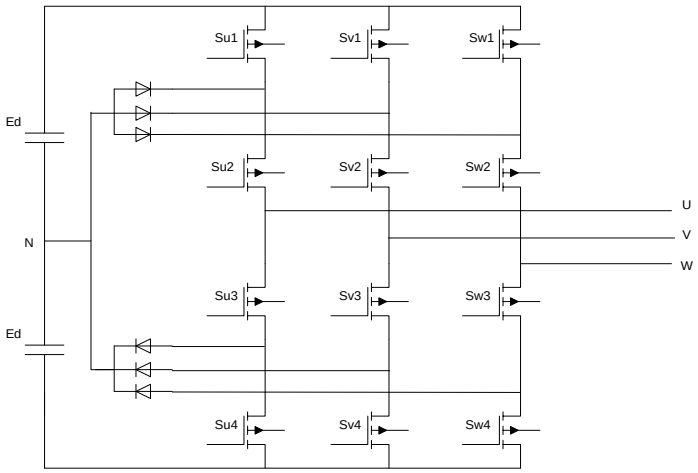

Figure 1 Three-Phase Three-Level Neutral Point Clamped Inverter.

$$\bar{I}_S = \frac{1}{2\pi}\int_0^{\pi} \sqrt{2}\, I_{rms} \sin(\omega t - \theta)\, dt \tag{3}$$

where θ is power factor :

$$\theta = \tan^{-1}(\frac{\omega L}{R}) \tag{4}$$

with assumption power factor is 1, the maximum mean value of current for each switch is 10 Ampere. With design factor 1.5 and low switching frequency, MOSFET IRFP460 is selected. The specification of this semiconductor switch are :

- Rated Voltage : 500 V
- Rated Current : 20 A
- $t_{d(on)}$: 50 ns

Then, clamping diode current rating is derived from equation below [1] :

$$I_D = \frac{1}{2} I_S \tag{5}$$

from equation (5), Fast diode S20L60 is selected with specification :

- Rated Voltage : 600 V
- Rated Current : 20 A
- $t_{d(on)}$: 100 ns

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III. PWM GENERATION USING FPGA

There are many modulation techniques and control paradigms that have been developed for three-level inverter, one of which is pulse width modulation (PWM). This technique offer a simplicity in controlling magnitude and frequency of the ac output voltages [5]. PWM is generated by comparing the reference signal with the carrier signal and as the result the output voltages wave form will resemble its reference signal. In this paper, there are two PWM schemes which are generated, these are sinusoid PWM and third harmonic injection PWM.

Modulation signal is generated by Altera DE2-70 development board, which will be implemented at three-level inverter. Designers could probably use schematic design or program with verilog or VHDL programming language based to design and meet the required specification. The specification of the design is :

Table 1 Modulation signal specification.

Modulation Index	0,00 – 2,00
Frequency	0 – 60 Hz
Carrier Frequency	1 kHz
PWM Mode	3 Mode
Output	12 bits PWM pulse, and display
Sampling Frequency	1 MHz
Dead time	2us
Voltage ON/Off	3,3 Volt / 0 Volt

There are three main inputs that determine the output of this PWM generation, these are frequency, modulation index, and PWM mode. These inputs can be set according to user desires. PWM mode determine which reference signal is used (pure sine, sine with 1/4 harmonic injection, or sine with 1/6 harmonic injection). Frequency set the actual frequency of the reference signal while modulation index set the magnitude of the reference signal.

Fig. 2 shows how PWM generation works. Sine wave is generated using CORDIC (Coordinate Rotation Digital Computer) algorithm that depend on frequency and modulation index as its inputs [6].

Then by the same way 3rd harmonic sine wave is generated but with different frequency and modulation index in accordance with PWM mode used. The sum of the two produces a reference signal which will be compared with a carrier signal later. If PWM mode is in pure sine mode, then the reference signal is pure sine wave without adding the 3rd harmonic sine wave. Carrier signal is generated by using a lookup table for a half of its period and by using counter up and down, the remaining half period value which is stored in lookup table is recalled. Then this signal is given a positive and negative offsets to obtain a double carrier signal. Finally, the compared signal is passed to the dead time module to avoid short circuit caused by two switch which conducts together. Dead time is made by using D-flipflop to delay the "ON" timing of the pulse.

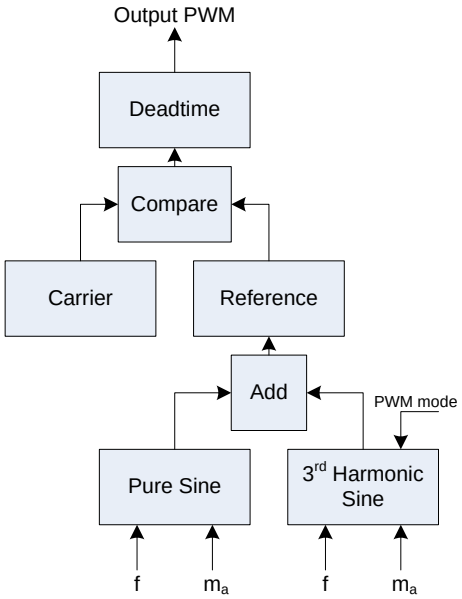

Figure 2 PWM generation scheme.

IV EXPERIMENTAL RESULT

Output wave form test is done by measure the line voltage. Line voltage is obtained by make four output pins become two output pins in one leg by adding AND logic functions. This line voltage wave form is surely brings high harmonics, hence it needs a filter to pass low frequency to the measurement instrumentation. The low-pass filter that used is using 225 Hz cut-off frequency. Fig. (3 – 5) below show the output wave form which resemble its reference signal. It can be concluded that the PWM generation is correct.

Index modulation test is done by looking at the relationship between inverter ac output voltages and index modulation. Fig. 6 shows that increment of index modulation affects in increasing output voltages linearly. Its also shown that harmonic injection signal is not influential in phase voltages, because they cancel each other.

In order to verify recent research about minimization of output current ripple experiment is done. A dead time of 2 μs was used to prevent a short circuit through the upper arm and lower arm. Load that is used in these experiments is a static load with resistance R = 20Ω and inductance L = 6.4 mH.

In this experiment, the dc source voltage, Ed = 50 V, was obtained by using a three-phase diode bridge rectifier.

To reduce the effects of the rectifier output harmonics on the investigated inverter, a capacitor having a large capacitance (4600 μF) was connected in parallel with the output terminals of rectifier. The inverter was operated at low switching frequency (1000 Hz) to reduce the dead-time effects in the experimental results.

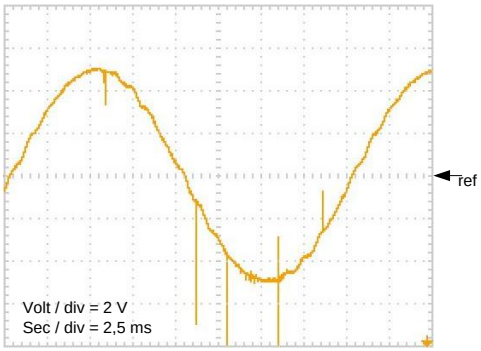

Figure 3 Pure sine wave

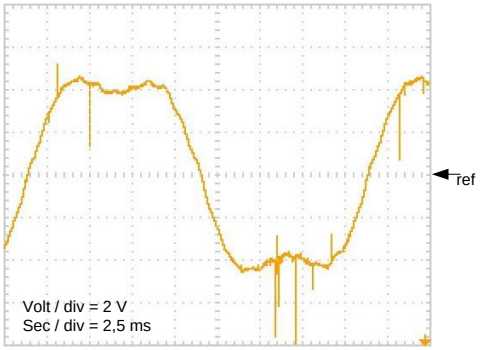

Figure 4 Sine wave with 1/4 3rd harmonic injection.

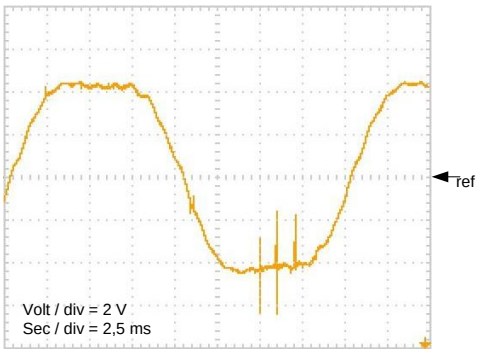

Figure 5 Sine wave with 1/6 3rd harmonic injection.

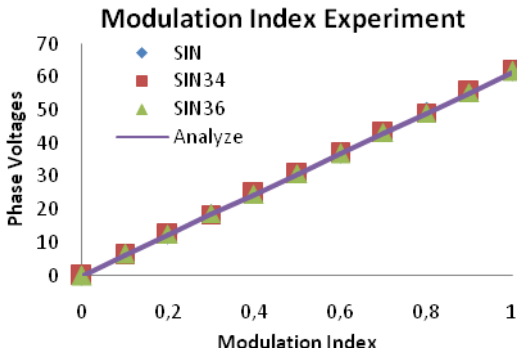

Figure 6 Modulation index experiment.

In order to measure the total harmonic, the inverter output current waveform during one fundamental period is recorded by using a digital storage oscilloscope. The data in the oscilloscope are subsequently analyzed by a computer to determine the total harmonic.

Figure 7 shows total output current ripple as a function of modulation indeks. Figure 7(a) shows total output current ripple under sinusoidal reference signal. Fig. 7(b) shows total output current ripple under sinusoidal plus 1/4 third harmonic injection. Fig. 7(c) shows total output current ripple under sinusoidal plus 1/6 third harmonic reference signal. Fig. 7(d) shows total output current ripple compared with each modulation techniques. Although the difference is very small, the output current ripple under sinusoidal plus 1/4 third injection is minimum at modulation index 0-0.8 and minimum at modulation indeks 0.8-1 under sinusoidal plus 1/6 third harmonic injection.

IV. CONCLUSION

Three-Phase Three Level Inverter is designed and recent research about minimization of output current ripple is verified. The output current ripple can be minimized by injecting third harmonic into modulation signal. The output current ripple under sinusoidal plus 1/4 third injection is minimum at modulation index 0-0.8 and minimum at modulation index 0.8-1 under sinusoidal plus 1/6 third harmonic injection.

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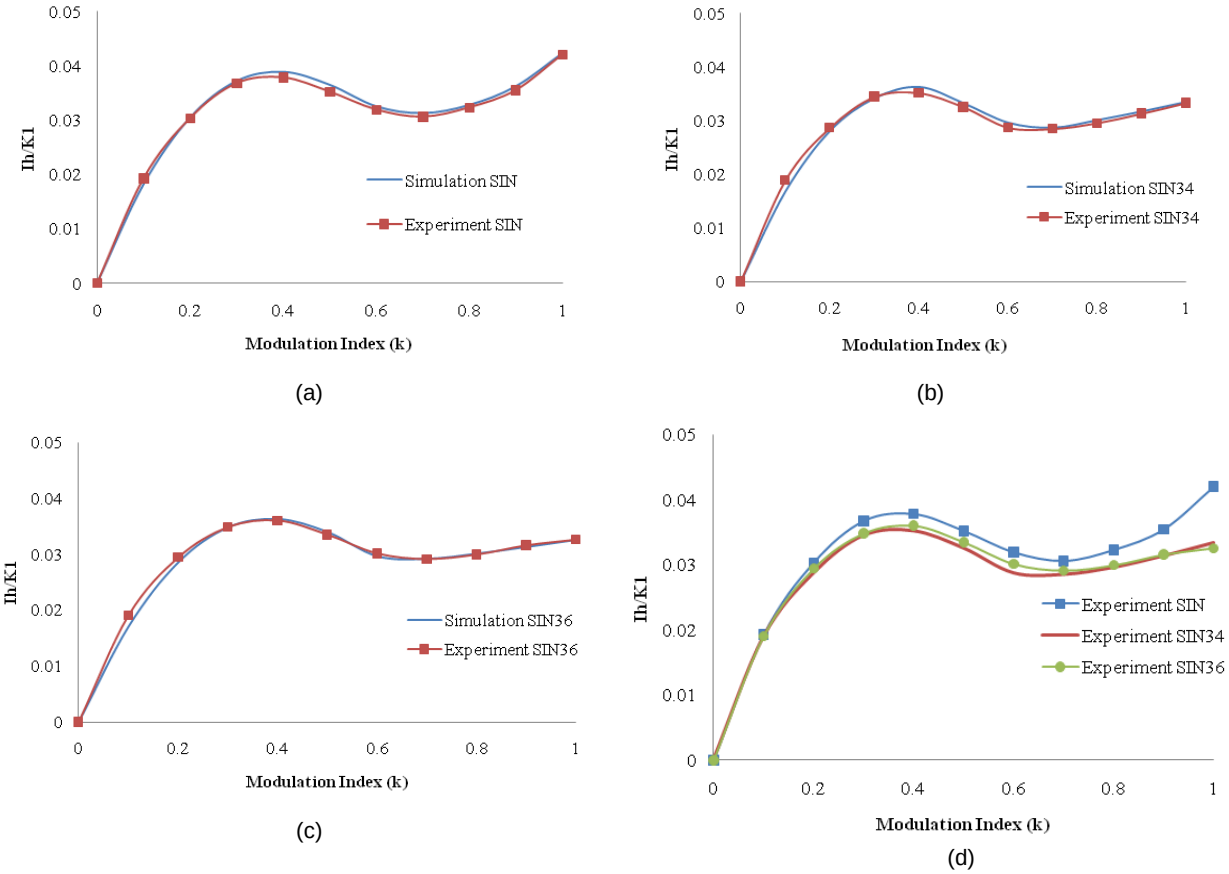

Figure 7 Total output current ripple as a function of modulation index. (a) under sinusoidal references (b) under sinusoidal plus 1/4 third harmonic injection (c) under sinusoidal plus 1/6 third harmonic injection (d) comparation of each modulation techniques